	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	308849	doped or doping or "p-type" or "n-type" or phosphorous	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:14
2	BRS	L2	109113	polysilicon or "polycrystalline silicon"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:14
3	BRS	L3	15744	getter$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:14
4	BRS	L4	113	(doped or doping or "p-type" or "n-type" or phosphorous) with (polysilicon or "polycrystalline silicon") with getter$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:14
5	BRS	L5	607104	trench or recess	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:15

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L9	2094	(doped) same polysilicon same LPCVD	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:15
7	BRS	L10	0	((doped) same polysilicon same LPCVD) and (getter$3 adj3 plug$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:15
8	BRS	L12	0	polysilicon with LPCVD with dop$3 with phophorus	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:15
9	BRS	L13	916	polysilicon with LPCVD with dop$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:15
10	BRS	L16	0	(getter$3 adj3 plug) with polysilicon with dop$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:15

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L17	0	(getter$3 adj3 plug) with polysilicon	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:15
12	BRS	L6	21	((doped or doping or "p-type" or "n-type" or phosphorous) with (polysilicon or "polycrystalline silicon") with getter$3) and (trench or recess)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:16
13	BRS	L7	12	(((doped or doping or "p-type" or "n-type" or phosphorous) with (polysilicon or "polycrystalline silicon") with getter$3) and (trench or recess)) and phosphorus	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:16
14	BRS	L11	49	((doped) same polysilicon same LPCVD) and getter$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:16
15	BRS	L14	334	(polysilicon with LPCVD with dop$3) and phosphorous	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:16

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L15	6	((polysilicon with LPCVD with dop$3) and phosphorous) and getter$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:16
17	BRS	L18	75	(getter$3) with polysilicon with dop$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:16
18	BRS	L19	1	(getter$3) with polysilicon with dop$3 with LPCVD	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:16
19	BRS	L20	69	polysilicon with (dop$3) with LPCVD with (cavity or cavities or hole or holes or trench or trenches or aperture or apertures or recess or recesses)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 18:16

US-PAT-NO: 6429481

DOCUMENT-IDENTIFIER: US 6429481 B1

TITLE: Field effect transistor and method of its manufacture

---------- KWIC ---------

Preferred embodiments include one or more of the following features. The first
dopant comprises arsenic and the second dopant comprises **phosphorus**. The first
energy is from about 80 to 120 keV. The first dosage is from about 5E15 to
1E16. The second energy is from about 40 to 70 keV. The second dosage is from
about 1E15 to 5E15. The resulting depth of the source is from about 0.4 to 0.8
.mu.m in the finished DMOS transistor.

Next, as shown in FIG. 4e, polysilicon is deposited to fill the trench and
cover the surface of the substrate, generally to a thickness of from about 1 to
2 .mu.m depending on the trench width (shown by the dotted lines in FIG. 4e).
This layer is then planarized by the nature of its thickness relative to the
trench width, typically from about 2 to 5 k.ANG.
(indicated by solid lines in
FIG. 4e). The polysilicon is then doped to n-type, e.g., by conventional
POCL.sub.3 doping or by **phosphorus** implant. The backside of the wafer need not
be stripped (as is conventionally done prior to **doping the polysilicon** to
enhance defect gettering) because any further doping of the highly doped
substrate would be unlikely to result in any enhancement in defect gettering.

The n+ source regions and n+ contact are then formed using a double implant.

For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of 5E15 to 1E16 followed by a second implant of **phosphorus** at an energy of 40 to 70 keV and a dose of 1E15 to 5E15. The **phosphorus** implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. **Phosphorus** ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8 .mu.m after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts 16 (see FIGS. 1 and 1a) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. 5a and 5b, respectively.

US-PAT-NO: 6140175

DOCUMENT-IDENTIFIER: US 6140175 A

TITLE: Self-aligned deep trench DRAM array device

---------- KWIC ---------

FIG. 2 shows a thin capacitor node dielectric 20 formed using SiN growth and/or deposition (LPCVD), and a re-oxidation. The **trench** 13 is filled with **doped polysilicon** 21 using, for example, **LPCVD**. In FIG. 3, the doped polysilicon 21 is planarized to the wafer surface using, for example, chemical mechanical polishing (CMP) or dry etching. Then the doped polysilicon 21 is recessed using a dry etch combination containing for example, SF.sub.6, CF.sub.4, HBr, to a depth of 0.8 um to 1.5 um below the surface of the pad SiN 12.

US-PAT-NO: 5677222

DOCUMENT-IDENTIFIER: US 5677222 A

TITLE: Method for forming a DRAM capacitor

---------- KWIC ---------

A doped polysilicon layer 232, shown in FIG. 15, is then formed on the
dielectric layer 228. A **LPCVD** process is used to deposit the **doped polysilicon**
layer 232 formed on the dielectric layer 228 so as to fill the **trench** 231 and
the rounded **cavities**. The doped polysilicon layer 232 is doped using P.sup.31
at a concentration of about 1E21 atoms/cm.sup.2 to increase conductivity.

US-PAT-NO: 6268627

DOCUMENT-IDENTIFIER: US 6268627 B1

TITLE: Semiconductor device having impurity regions with varying impurity
concentrations

---------- KWIC ---------

Now with reference to FIG. 12, a **polysilicon** film **doped** with phosphorus (not
shown) is formed on silicon oxide film 13 by the **LPCVD** to fill in contact **holes**
14a, 14b, and 14c. The film has a thickness of 1000 to 2000 .ANG. and its
phosphorus concentration is 1.0.times.10.sup.20 to 8.0.times.10.sup.20
/cm.sup.3. A prescribed photoresist pattern (not shown) is then formed on the
polysilicon film by photolithography. Using the photoresist pattern as a mask,
the phosphorus-doped polysilicon film is etched by the RIE, thereby forming
interconnections 15a and 15b. Impurity regions 12b, silicon oxide film 13 and
interconnection 15b constitute a p channel type TFT (Thin Film Transistor) as a
load element of the memory cell in an SRAM, respectively serving as its channel
region, gate insulating film and gate electrode. FIG. 13 shows a planar
structure of the memory cell at this manufacturing step, and FIG. 12 is a
sectional structure taken along the line A--A in FIG. 13.